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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
SCS-550-489	

Application Number	Filed
10/715,368	November 19, 2003
First Named Inventor: FLYNN	
Art Unit: 2116	Examiner: M. Brown

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 27,393 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1.34 _____

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June 13, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

STATEMENT OF ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

The following listing of clear errors in the Examiner's rejection and his failure to identify essential elements necessary for a *prima facie* basis of rejection is responsive to the fifth and non-final Official Action mailed March 13, 2008 (Paper No. 20080225). It is noted that the newly cited Tobias reference is no more pertinent than the previously cited Kobayashi reference as discussed in the Pre-Appeal Brief Request for Review filed November 26, 2007 (the Panel decided to reopen prosecution on December 20, 2007).

Error #1. The Examiner still ignores the limitations of independent claims 1, 6 and 11

Each of independent claims 1, 6 and 11 specifies that the "at least one further circuit" has an interrelationship with the processor so as to support "data processing of said processor at **at least one intermediate data processing performance level . . . during said change**" (emphasis added). In the 5th and non-final rejection, page 3, section 3, the Examiner admits that the Cooper reference fails to disclose the claimed "at least one further circuit." In the latest admission, the Examiner now includes a significant portion of each of the independent claims, i.e., the portion specifically stating the interrelationship which is supported by the further circuit, i.e., "supports data processing of said processor at at least one intermediate data processing performance level during said change" [the change from a first desired data processing performance level to a second desired data processing performance level]. The Examiner now appears to appreciate that Applicant's independent claims 1, 6 and 11 all positively recite this interrelationship is clear evidence of error on the Examiner's part in his prior attempts to read prior art on the pending claims.

The Examiner now cites Tobias (USP 7,254,721) as teaching "data processing of said processor at at least one intermediate data processing performance level . . . during said change" having admitted that Cooper fails to contain any such teaching. As will be seen, Tobias also fails to contain any teaching and that, combined with the fact that Cooper actually teaches "quiescence" between performance states, teaches away from any such disclosure and obviates the Examiner's rejections.

Error #2. The Examiner misunderstands the Tobias reference teaching

In the paragraph bridging pages 3 and 4 of the 5th and non-final Official Action, the Examiner alleges that Tobias teaches that "said processor temporarily operates at said at least one intermediate data processing performance level during said change" and cites Tobias at column 4, line 64 to column 5, line 31. Both the conclusion and the reference are inaccurate and incorrect.

The cited portion of Tobias actually suggests that

> "the power management selects the maximum performance state P5 as the next performance state. Thus, if the performance state is always taken straight to the maximum performance state when a performance increase is required . . . there is less of a chance that a user could notice any performance degradation." (Column 5, lines 19-27). Similarly, "if a lower performance state is required, a next lower performance state is selected." (Column 5, lines 32-33).

Thus, Tobias clearly teaches that one sequentially steps from P1 to P2 to P3 to P4 to P5 when increasing and similarly when decreasing processor speeds. This is accomplished in Tobias because performance level is selected by controlling a programmable voltage ID (VID) field or core clock frequency control field (see the discussion at column 11, lines 54-58).

Importantly, Tobias, when changing performance levels, issues a "stop grant" signal to indicate to the CPU core that the CPU core should stop execution of operating system and application code and **enter a stop grant state** (Tobias, column 11, line 54 through column 12, line 3). During the "stop grant state," a new VID value is sent to a voltage regulator and the new clock frequency control value

is supplied to the clock generation circuit (Tobias, column 13, lines 63-66). In Tobias, once the new clock frequency and the new voltage have been stabilized, then the stop signal is deasserted and the CPU core resumes executing code (Tobias, column 14, lines 1-8).

Thus, in view of the above, Tobias clearly requires that the CPU not operate during performance level changes since it implements the "stop grant state." Thus, Tobias, like Cooper's "quiescent" state, requires a "stop grant state" in which the CPU does not operate "during said change" in data processing performance level. As a result, neither Cooper nor Tobias teach the feature of Applicant's independent claims, i.e., the claimed "at least one further circuit" which supports data processing at an intermediate data processing performance level "during said change."

Error #3. The Examiner errs in failing to identify any "reason" or "motivation" for combining Cooper and Tobias

In the partial paragraph at the top of page 4 of the 5th Official Action, the Examiner alleges that it would have been obvious to "add Tobias' power management control logic 507 to Cooper's system for adjusting CPU performance." The Examiner suggests that the motivation "to do so would be to reduce the chance that any degradation is detected by a system user" and cites Tobias column 5, lines 40-41. However, the motivation discussed at the cited portion of Tobias is with respect to the stepwise changing of performance level from step P5 to P4 then to P3 then to P2, etc. It is this stepwise performance change that Tobias uses to "reduce the chance that any degradation is detected by a system user."

The Examiner does not identify any teaching in either Cooper or Tobias which suggests processor operation at any intermediate data processing level "during said change," i.e., from P2 to P3 or vice versa. Given that the Examiner can't identify any disclosure of the operation "during said change," he certainly can't provide any rationale for picking and choosing elements from the Cooper

and Tobias references and then combining them in the manner of Applicant's independent claim 1. Accordingly, there is no *prima facie* case of obviousness under §103 over the Cooper/Tobias combination.

In accordance with the recent Supreme Court decision in *KSR v. Teleflex*, it is incumbent upon the Examiner to articulate some "reason" for picking and choosing elements from the various prior art references and then combining them in the manner of the claimed invention. The Supreme Court specifically indicated that the examiner's rationale must be made explicit ("to facilitate review, this analysis should be made explicit." *KSR International Co. v. Teleflex, Inc.* 82 USPQ2d 1385, 1396 (SCT 2007)).

Because the Examiner has failed to provide any reason for combining the Cooper and Tobias references, he has failed to establish a *prima facie* case of obviousness under 35 USC §103 with respect to independent claims 1, 6 and 11.

Error #4. The Examiner appears to ignore the fact that both Cooper and Tobias teach away from Applicant's claimed combination

As noted above, the Cooper reference clearly teaches away from Applicant's claimed "intermediate data processing level during said change" by teaching that the processor is in a "relatively quiescent state" during any such change. Tobias similarly requires, when changing power levels, the existence of the "stop grant state" so that the processor completes the last instructions and then stops.

Both the Cooper and Tobias references would lead one of ordinary skill in the art away from the claimed invention. The fact that both cited references would lead one of ordinary skill in the art away from the claimed invention which operates the processor at an intermediate performance level "during said change" is evidence which clearly rebuts any *prima facie* case of obviousness established

by the Examiner (even if the Examiner had made out a *prima facie* case and, as noted above, the Examiner has failed to establish such a case).

SUMMARY

Independent apparatus claim 1, method claim 6 and means-plus-function claim 11 all require a specific interrelationship between the "one further circuit" and the "processor." Cooper's teaching of a single processor going to a "quiescent" state while changing power levels and Tobias' teaching of a "stop grant state" when changing power levels fails to disclose any processor operation at any "intermediate data processing performance level during said change." The Examiner has failed to provide any "explicit analysis" as to why one would be motivated to combine portions of the two references in the manner of the independent claims and therefore fails to meet his burden of establishing a *prima facie* case of obviousness. Moreover, the Examiner fails to provide any evidence rebutting the fact conclusion that both references would lead one of ordinary skill in the art away from the claimed invention, thereby rebutting any *prima facie* case of obviousness.

As a result of the above, there is simply no support for the rejection of Applicant's independent claims 1, 6 and 11 or claims dependent thereon under 35 USC §103. Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution on the merits should be closed.